Problem 3

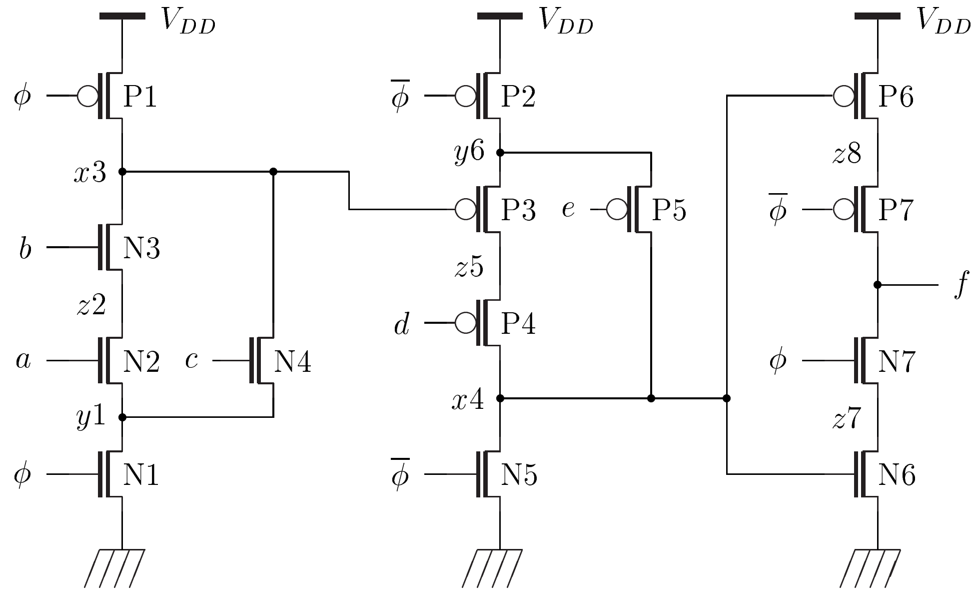

Figure 3: Transistor diagram of dynamic circuit

In this problem, the design of a dynamic CMOS circuit is considered. Figure 3 shows the transistor diagram of the circuit. In the diagram, ϕ denotes the clock, while a, b, c, d, and e are inputs to the circuit. The supply voltage is $V_{DD} = 3V$.
In the layout, minimal geometries are used. The transistor sizes are (W,L)=(2.5μm,1μm). Furthermore, internal routing capacitances are approximated by a 20μm long metal-1 wire over substrate for a connection between any two points. The load on the output node f is approximated by an additional 30μm long metal-2 wire over substrate.

Question 3.1

Explain, how the circuit in Figure 3 works, and write down the function realized.
Describe the requirements on the inputs a, b, c, d, and e in order to make the logic insensitive to glitches.

Question 3.2

Calculate the capacitances of the internal nodes $z2$, $z5$, $z7$, $z8$, $y1$, $y6$, $x3$ and $x4$, and the output node f.
Calculate the effective resistances R_n and R_p of n-channel and p-channel transistors, respectively, operating in the linear region.

Question 3.3

Draw an RC-model of the circuit for calculation of the worst-case delays t_{dr} and t_{df}, which may occur during a logic shift of the output f, and calculate the variables of the model.
Calculate the worst-case delays t_{dr} and t_{df}.

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Appendix 1: 1.0μm CMOS process parameters and design rules

Film thickness		
Gate oxide thickness	t_{ox}	200 Å
Field oxide thickness	t_F	5000 Å
Oxide thickness between poly and metal-1	t_{mp}	7000 Å
Oxide thickness between metal-1 and metal-2	t_{mm}	12000 Å
Thickness of polysilicon layer	t_p	4000 Å
Thickness of metal-1 layer	t_{m1}	6000 Å
Thickness of metal-2 layer	t_{m1}	10000 Å
Junction depth p^+/n^+ diffusion	x_j	4000 Å
Junction depth n-well diffusion	x_w	30000 Å
Depletion layer thickness pn junction	x_d	3000 Å
Depletion layer thickness under channel	x_k	3000 Å

Transistor parameters		
Current factor $[\mu A/V^2]$	KP_n	98
	KP_p	38
Threshold voltage $[V]$	V_{tn0}	0.8
	V_{tp0}	- 0.8
Body effect coefficient $[\sqrt{V}]$	γ_n	0.75
	γ_p	0.75
Bulk potential $[V]$	ϕ_{bn}	0.37
	ϕ_{bp}	- 0.37
Channel length modulation $[V^{-1}]$	λ_n	0.01
	λ_p	0.038

Capacitances		Area $fF/\mu m^2$		Perimeter $fF/\mu m$	
metal-2	to substrate	C_{m2}	0.017	C_{m2p}	0.052
metal-1	to substrate	C_{m1}	0.029	C_{m1p}	0.046
poly	to substrate	C_p	0.058	C_{pp}	0.055
n^+ diffusion (0V)	to substrate	C_{jn}	0.40	C_{jnp}	0.52
p^+ diffusion (0V)	to substrate	C_{jp}	0.62	C_{jpp}	0.87
gate capacitance		C_{ox}	1.95		—