Solution to supplementary problems.

Problem 12

Resistances and capacitances of a $100\mu m$ long minimum width conductor calculated using 0.18 micron design rules:

$$R = \frac{L}{W} \cdot R_{\square} \qquad C = L \cdot W \cdot C_{ja} + 2 \cdot (L + W) \cdot C_{jp}$$

The result are listed below. However, the design rules do not specify a perimeter dependent value, C_{jp}, for any layer. For a minimum width conductor, the capacitances are dominated by the contributions from the perimeters. For such a conductor, it is possible to reduce the RC time constant by increasing the conductor width. This would lower R without changing C accordingly.

Problem 12	Poly	Metal1	Metal2	Metal3	Metal4	Metal5	Metal6
W $[\mu m]$	0.18	0.32	0.32	0.32	0.32	0.64	0.64
$R_{\square}$ $[\Omega/\square]$	108	$72m$	$72m$	$72m$	$72m$	$35m$	$35m$
C_{ja} $[aF/\mu m^2]$	93.3	22.4	12.6	8.77	6.72	5.45	4.34
R $[\Omega]$	$60k$	22.5	22.5	22.5	22.5	5.47	5.47
C $[aF]$	1680	717	403	281	215	349	278

Problem 13	Poly	Metal1	Metal2	Metal3	Metal4	Metal5	Metal6
W $[\mu m]$	0.18	0.32	0.32	0.32	0.32	0.64	0.64
r $[\Omega/\mu m]$	108	$72m$	$72m$	$72m$	$72m$	$35m$	$35m$
c $[aF/\mu m]$	16.8	7.17	4.03	2.81	2.15	3.49	2.78
ℓ $[mm]$	0.198	11.8	15.7	18.8	21.5	24.2	27.1

Problem 13

The delay of a long, unloaded conductor, applying a step function at the input, calculated using resistance per unit length, r, and capacitance per unit length, c:

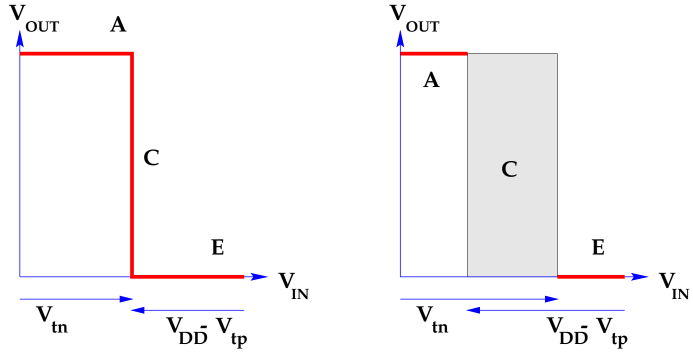
$$\tau = 0.7\,\frac{rc\ell^2}{2} \Leftrightarrow \ell = \sqrt{\frac{2\tau}{0.7 \cdot rc}} \qquad r = \frac{R_{\square}}{W_{min}} \qquad c = W_{min} C_{ja} \quad (C_{jp} = 0)$$

The result are listed in the Table above.

Problem 14

a)

	p-device	*n-device*
A	**linear**	**cut-off**
C	**saturated**	**saturated**
E	**cut-off**	**linear**



The region of operation is indicated in figure above along with the inverter characteristics for the case $V_{DD} = V_{tn} - V_{tp} = V_{tn} + \mid V_{tp} \mid$. Note that the current in the vertical region (labeled 'C') is zero, i.e. the shifting takes place in the horizontal regions (labeled 'A' and 'E', respectively. Therefore, the *short-circuit* component, $P_{short-circuit}$, of the total power consumption, $P_{total} = P_{static} + P_{dynamic} + P_{short-circuit}$, disappears for low supply voltages, $V_{DD} \leq V_{tn} - V_{tp}$.
For values of V_{DD} below $V_{tn} - V_{tp}$, the characteristics are shown in the figure. As before, in region 'A' ('E'), the n-channel is cut-off (linear), and the p-channel transistor is linear (cut-off). The inverter action takes place in regions 'A' and 'E'. In the interval $[\ V_{DD} + V_{tp}; V_{tn}\ ]$ (region 'C'), the output is high-impedant.
$V_{DD,min}$ is determined by the requirement, that both transistors can conduct current:

$$\{\ V_{DD} - V_{tn} > 0 \quad \wedge \quad -V_{DD} - V_{tp} < 0\ \} \quad \Leftrightarrow \quad V_{DD} > max\ \{\ V_{tn}; -V_{tp}\ \}$$

b)

The lower limit on the supply voltage, $V_{DD,min}$, was determined in the previous question:

$$V_{DD} > max\ \{\ V_{tn}; -V_{tp}\ \}$$

For voltages above this minimum, the series connection will pull up the output node. For very low supply voltages, transistor P2 may be cut off due to body effects at the onset of the shift. Eventually, the source of P2 will be pulled up, and P2 conducts.
This worst-case situation is depicted in the figure to the right. Initially, P2 will be cut-off, next saturated, and finally, linear. Accordingly, the calculation of t_{dr} will be divided into three terms.
For larger values of V_{DD}, only the two later terms are relevant.